void \_clockInit72(void)

{

/\* Enable HSE (HighSpeedExternal)\*/  
RCC->CR |= RCC\_CR\_HSEON;

/\* Wait for HSE to become ready \*/

while ((RCC->CR & RCC\_CR\_HSERDY) == 0);

/\*

\* Configure Main PLL

\* HSE as clock input

\* HSE = 8MHz

\* fpllout = 72MHz

\* PLLMUL = 9

\* PLL configuration is really straight forward. Setting the PLLMULL bits in the

\* RCC->CFGR to 0b0111 results in a multiplication factor of 9.

\* Select the HSE as PLL source by setting the PLLSRC bit in the configuration register.

\* See chapter 8.3.2 in the manual for more information.

\*/

RCC->CFGR = (0b0111 << 18) | RCC\_CFGR\_PLLSRC;

/\* PLL On \*/

RCC->CR |= RCC\_CR\_PLLON;

/\* Wait until PLL is locked \*/

while ((RCC->CR & RCC\_CR\_PLLRDY) == 0);

/\*

\* FLASH configuration block

\* enable instruction cache

\* enable prefetch

\* set latency to 2WS (3 CPU cycles)

\*/

FLASH->ACR |= FLASH\_ACR\_PRFTBE | FLASH\_ACR\_LATENCY\_2;

/\* Set HCLK (AHB) prescaler (DIV1) \*/

RCC->CFGR &= ~(RCC\_CFGR\_HPRE);

/\* Set APB1 Low speed prescaler (APB1) DIV2 \*/

RCC->CFGR |= RCC\_CFGR\_PPRE1\_DIV2;

/\* SET APB2 High speed prescaler (APB2) DIV1 \*/

RCC->CFGR &= ~(RCC\_CFGR\_PPRE2);

/\* Set clock source to PLL \*/

RCC->CFGR |= RCC\_CFGR\_SW\_PLL;

/\* Busy-wait until PLL is active as clock source \*/

while ((RCC->CFGR & RCC\_CFGR\_SWS\_PLL) != RCC\_CFGR\_SWS\_PLL);

SystemCoreClock = 72000000UL;

}